METHOD AND STRUCTURE FOR REDUCING GATE LEAKAGE AND THRESHOLD VOLTAGE FLUCTUATION IN MEMORY CELLS

ABSTRACT OF THE DISCLOSURE

A memory device has a memory cell including a plurality of active devices, which can be switched on by an applied threshold voltage. A power line is coupled to at least one storage node by one of the active devices. One other of the active devices couples a virtual ground to the storage node. Potentials of the power line and the virtual ground cause the plurality of active devices to be selectively operated in near subthreshold and/or superthreshold regimes in accordance with a mode of operation.